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Area & Power Optimized Hybrid CMOS-Memristor Logic Circuit-Based Carry Look-Ahead Adder

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A B S T R A C T

Memristor, in addition to the well-known resistor, capacitor, and inductor, is the fourth fundamental two-terminal passive circuit component. Many researchers have recently suggested memristor-based architectures. Memristor-based digital logic circuits offer a possible replacement for traditional IC technology by creating new avenues for investigating cutting-edge computing designs. The memristor Ratioed logic (MRL) is compatible with conventional CMOS technology in a number of memristor-based logic design methodologies. On the basis of the hybrid CMOS-memristor structure, two types of carry-look ahead adders (CLA) are proposed, one of which is based on MRL logic and the other of which is an upgraded type that is implemented by MRL universal gate (MRLUG). The suggested design method uses a reduced number of memristors and CMOSs than IMP-based or CMOS-based CLAs, resulting in a smaller circuit size and less power consumption. The proposed CLAs are verified by theoretical analyses and simulations.

Index Terms Memristor, Memristor Ratioed Logic (MRL), Universal Logic Gate (ULG), CMOS, CLA

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1. INTRODUCTION

Moore's law predicts that the number of transistors doubles every 18 months. The exponential expansion of elemental devices could no longer be accommodated by integrated circuits (IC), much as modern CMOS transistors are running across miniaturization restrictions. Thus necessitating the creation of alternate circuit topologies that call for the least amount of CMOS transistors. New Nanoscale memory technology known as the memristor is a formidable rival for the next generation of computational frameworks [1].

A memristor is a 2-terminal circuit component that relates flux and charge q [2] [3]. The term "memory resistor" is the origin of the phrase "memristor." Memristor cannot store or produce any power because it is not an active component. Fig.1 depicts a memristor's symbol.

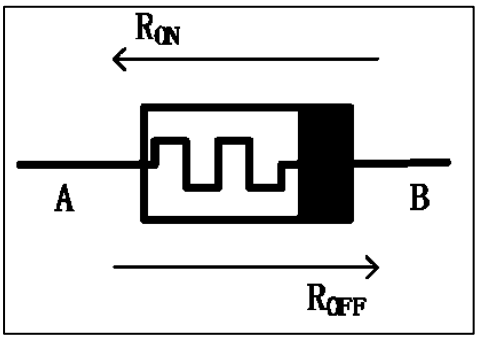

Fig. 1 Symbol of Memristor

The memristance fluctuates depending on the direction of the current. The memristor is represented by the dark side in Fig. 1, which stands for the device's negative polarity. The memristance increases to ROFF when the current runs from A to B, but it lowers to RON when the current flows from B to A.

Memristor operation is based on the device's previous state or history. The memristor is seen as a variable resistor with variable resistance as the device's memristance M. The amount of total current that flows through the device affects the memristor's M memory resistance. The memristor preserves its state after the voltage or current is removed from the source, and by using a lower voltage or current, the previous state can be easily read.

Memristors offer an unconventional architecture for computation that combines logic operation and memory-based storage [5]. Memristor-based logic circuits offer a fresh approach to investigating cutting-edge computer systems as an exciting replacement for conventional logic circuits.

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As a result, a number of memristor-based logical circuit design techniques have been proposed. A simple circuit made up of memristors and resistors can realize the material implication logic operation (IMP), which can then be combined with the FALSE operation to create a computationally complete logic unit and enable the operation of any Boolean logic function, according to a paper published by HP laboratories in 2010 [1]. A basic circuit for IMP operation may be found in Fig. 2, which includes two memristors (P and Q) and a load resistor (RG). The resistances of P and Q serve as the structure's logical variables, and a logic level of 1 corresponds to a low resistance state (RON), and a level of 0 to a high resistance value (ROFF). Applying voltages VCOND and VSET to P and Q, respectively, allows for the computation of the imply operation. It should be noted that P and Q serve as the input memristors at the start of the operation, and Q serves as the output memristor at the end of the operation (although the input value of Q may be lost)

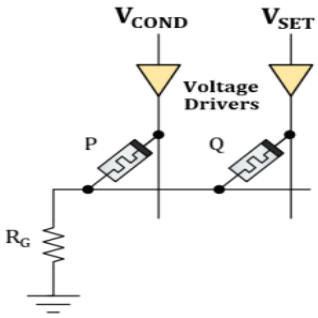

Fig. 2 Circuit Implementation of IMP operation

The symbol and truth table for IMP operation is shown in Fig. 3(a) and 3(b). The p IMP q can be written as "p → q" in a logical expression, and the material implication is regarded as a truth function in logic. However, the IMP logic's primary flaw is its inability to execute lengthy sequences.

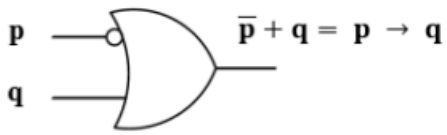

Fig. 3 (a) Symbol of IMPLY logic gate

p	q	p → q
0	0	1
0	1	1
1	0	0
1	1	1

b) Truth table of Implication operation

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Any logic function is said to be possible using memristors and conventional CMOS buffers, according to the memristor Ratioed logic (MRL) gate design method [6]. Voltage levels that are compatible with contemporary CMOS technologies make up the logic states. Several computational building blocks, including the multiplier [7], ripple carry adder [8], full adder [9], and oscillator [10], have been proposed in recent years.

In this paper, a carry look-ahead adder (CLA) based on MRL is first suggested, and subsequently a better carry look-ahead adder is advanced. The enhanced CLA has been compared to other CLAs in terms of performance, and this has been debated. Regarding the structure of this paper, Section II introduces the memristor model. Section III describes Memristor Ratioed Logic & implementation of logic gates using MRL. The carry look-ahead adder, which is found in Section IV, uses MRL logic. The enhanced carry look-ahead adder can be found in Section V. The conclusion is in Section VI.

II. MEMRISTOR MODEL

A suitable model is required to be able to develop, examine, and simulate memristor-based circuits and applications. Several models have been put forth since HP Labs' paper on memristor implementation was published in May 2008.

Based on the device's physical structure, the linear ion drift model is depicted in the Fig. 4(a). It is presumable that the D-width physical device has two regions. With positive oxygen ions doped on one side and none on the other. A resistor serves as the model for each region. The w-width doped region, which serves as the state variable, has less resistance and is hence more conductive. The undoped region also has a high resistance. Additionally, it is assumed that the field is uniform, ohmic conductance, the ion drift is linear, and the ions have equal average ion mobilities.

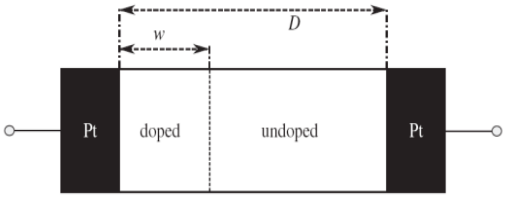
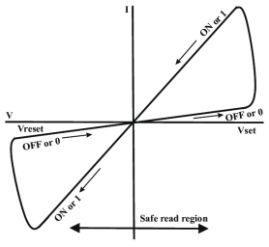


Fig. 4(a) Structure of Memristor



(b) I – V Characteristics of Memristor

The memristor's i-v characteristic curve is shown in Fig. 4(b). The memristor has several threshold voltages, and the various polarities of the voltages correlate to the various threshold voltages. The memristance will change from the HRS (High Resistance State) to the LRS (Low Resistance State) when the applied voltage surpasses the positive threshold value. Similar to this, the memristance

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from the LRS to the HRS will change when the applied voltage exceeds the negative threshold voltage.

III. MEMRISTOR RATIOED LOGIC (MRL)

Memristive and CMOS technologies are combined in the MRL (Memristor Ratioed Logic) family. MRL family devices use memristors to implement the AND and OR gates. The universal Boolean functions NAND and NOR can be generated by combining these gates with a CMOS inverter.

Fig. 5 OR & AND Gates using Memristor

The computing procedure is examined using the AND logic gate as an example. Two memristors are connected in series to form the logic AND gate. The output terminal is the common node of the two memristors, while the input terminal is connected to the positive polarity terminal of those two devices. The voltage divider of the two memristive devices controls the output voltage of the AND gate.

Four distinct input scenarios for the AND gate are shown in Fig. 6. Logic "1" is represented by Vcc, logic "0" is represented by 0 V, and input voltages V1 and V2 are used. In Fig. 6(a) and (b), A = B = 1 and A = B = 0, respectively, and as there is no current flowing from MR0 to MR1, the outputs are unchanged from the inputs. In Fig. 6(a), the input voltages are ground (logic "0"), and the output voltage is ground (logic "0") as well. In Fig. 6(b), the input voltages are Vcc (logic "1"), and the output voltage is Vcc (logic "1") as well.

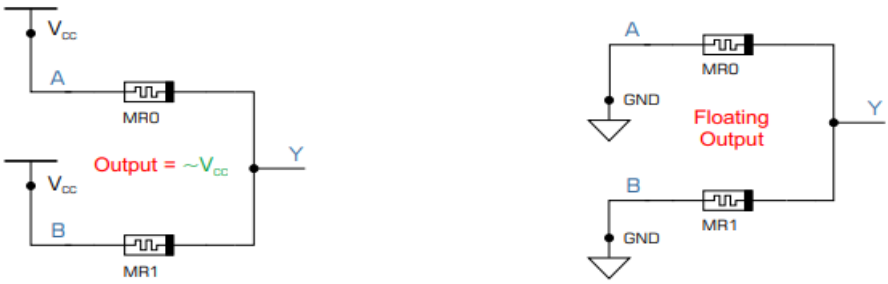

Fig. 6 Logical AND using Memristor a) Inputs A = 1, B = 1 b) Inputs A = 0, B = 0

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In Fig. 6(c), A = 1, B = 0, and the circuit has a current flowing from MR0 to MR1, causing the resistance of MR0 to rise to ROFF and that of MR1 to fall to RON. Assuming the voltage divider principle is used to determine the output voltage and ROFF > RON:

$$Y = VCC \times \frac{RON}{RON + ROFF} \approx 0$$

In Fig. 6(d), A = 0 and B = 1, and the circuit has a current flowing from MR1 to MR0. As a result, MR1's memristor experiences an increase in resistance to ROFF, and that of MR0 decrease in resistance to RON. Assuming the voltage divider principle is used to determine the output voltage and ROFF > RON:

$$Y = VCC \times \frac{RON}{RON + ROFF} \approx VCC$$

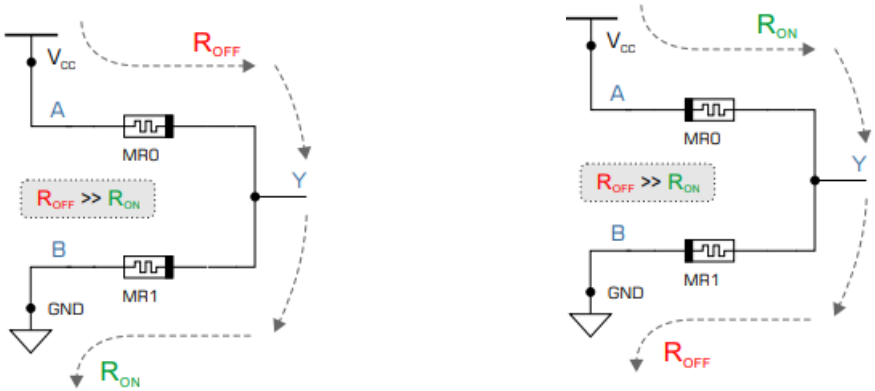

Fig. 6 Logical AND using Memristor c) Inputs A = 1, B = 0 d) Inputs A = 1, B = 0

It is possible to create additional logic gate circuits by combining conventional CMOS buffers. For instance, a NAND (NOR) logic gate can be created by combining an AND (OR) gate with a CMOS bufferas shown in the Fig. 7. It is also possible to construct other, more complicated combinational logic circuits, such the widely used XOR gates. The logic states of the MRL are voltage levels, similar to conventional logic circuits, unlike the implication logic circuits and MAGIC logic circuits. As a result, it works well with conventional logic circuits.

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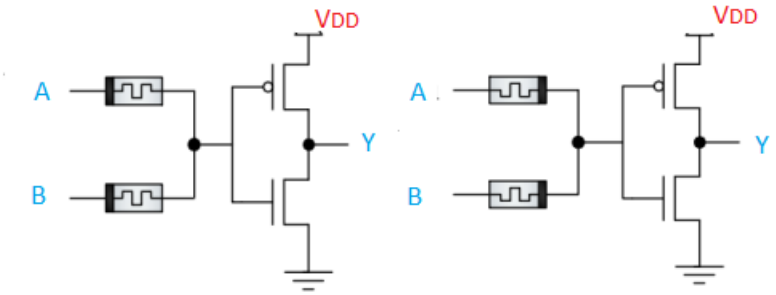

Fig. 7 NOR & NAND Gates using Memristor

IV. THE CARRY LOOK-AHEAD ADDER BASED ON MRL

A conventional carry adder is presented [12] to improve the multi-bit adder's operation speed and decrease transmission delays brought on by carry signal propagation. In ripple carry adders, the two bits that need to be added are always available for each adder block. On the other hand, each adder block awaits the previous block's carry. It is therefore impossible to generate the sum and carry of any block once the input carry has been established. While block n waits, block (n-1) generates the carry. Therefore, there will be a sizable time delay as a result of the carry propagation delay.

The carry look-ahead adder introduces two functions, namely the carry generates function Gi and the carry propagate function Pi.

$G_i = A_i B_i$ (1)

$P_i = A_i \oplus B_i$ (2)

The sum and carry output are given by

$S_i = P_i \oplus C_i$ (3)

$C_{i+1} = G_i + Pi\ C_i$ (4)

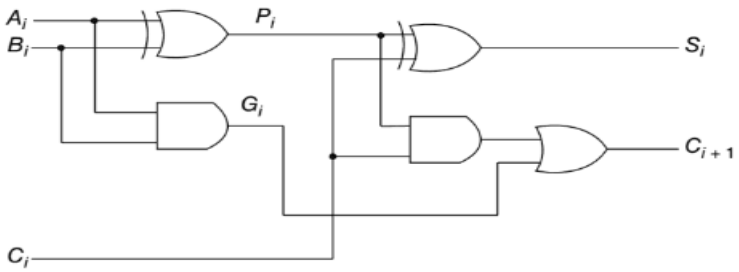

Fig. 8 Full adder circuit with Carry Generate and Carry Propagate

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Carry look-ahead adders are analogous to ripple carry adders. The distinction is that carry look-ahead adders can calculate the Carry bit before the Full Adder completes its operation. This provides it a benefit over the Ripple Carry Adder because it can add two digits faster. The block diagram of 4 bit Carry look-ahead adder is shown in Fig. 8.

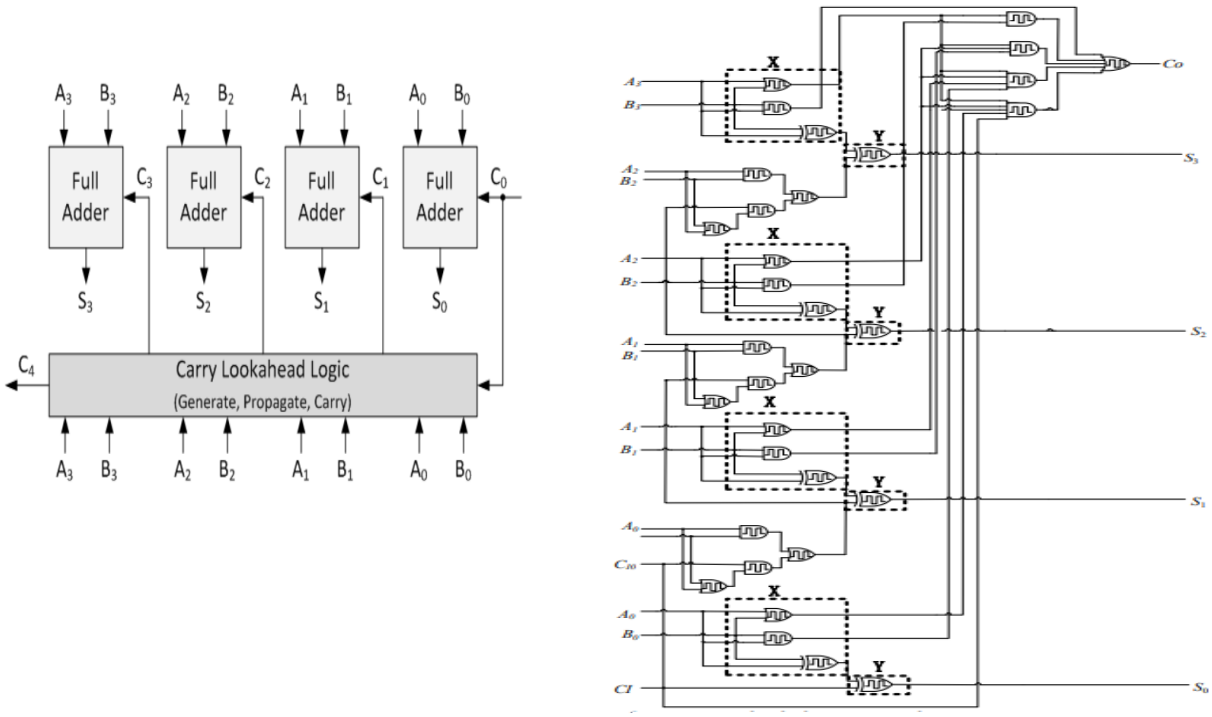

Fig. 9 (a) 4-bit Carry look-ahead adder (b) CLA implementation based on MRL

The circuit structure of a 4-bit carry look-ahead adder (CLA) based on MRL is provided in this research and may be seen in Fig. 9(b). A carry look-ahead adder is constructed using the MRL gate circuit and the carry output function and the output sum function. The circuit's XOR gate is a combinational logic gate made up of an AND gate and an OR gate. Additionally, the two input AND or OR gates are extended by the multiple input AND or OR gates.

V. ENHANCED CARRY-LOOKAHEAD ADDER

In [4], a new hybrid CMOS-memristor logic gate circuit referred to as a universal logic gate (ULG), is introduced. It uses an appropriate combination of MRL gates and a CMOS inverter. Fig. 10 displays the reduced circuit symbol and the circuit construction. The fundamental characteristic of

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this construction is that the input of the inverter is coupled with the output of the logic AND gate, the source of the PMOS is coupled with the output of the logic OR gate, and the output of the inverter just so happens to create an XOR gate.

The universal logic gate (ULG) performs the AND, OR, and XOR logic operations simultaneously using only 4 memristors and 2 CMOSFET transistors. Comparatively, the enhanced CLA uses two fewer memristors than an MRL-based XOR gate, which requires 6 of them. As a result, the integrated circuit architecture uses less space and power.

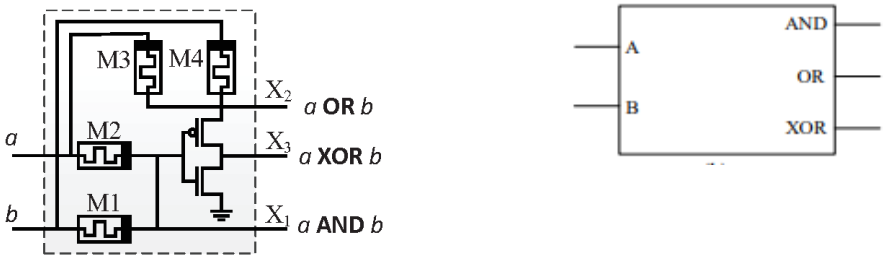

Fig. 10 (a) Circuit of ULG **(b) Symbol of ULG**

As seen in Fig. 6, the MRL-based CLA's dotted line block X, which includes an AND gate, an OR gate, and an XOR gate, can be substituted by a single ULG. Additionally, a ULG may be used in place of the CLA's dotted line block Y. So, as shown in Fig. 11, an enhanced MRL-based CLA circuit with ULGs is obtained.

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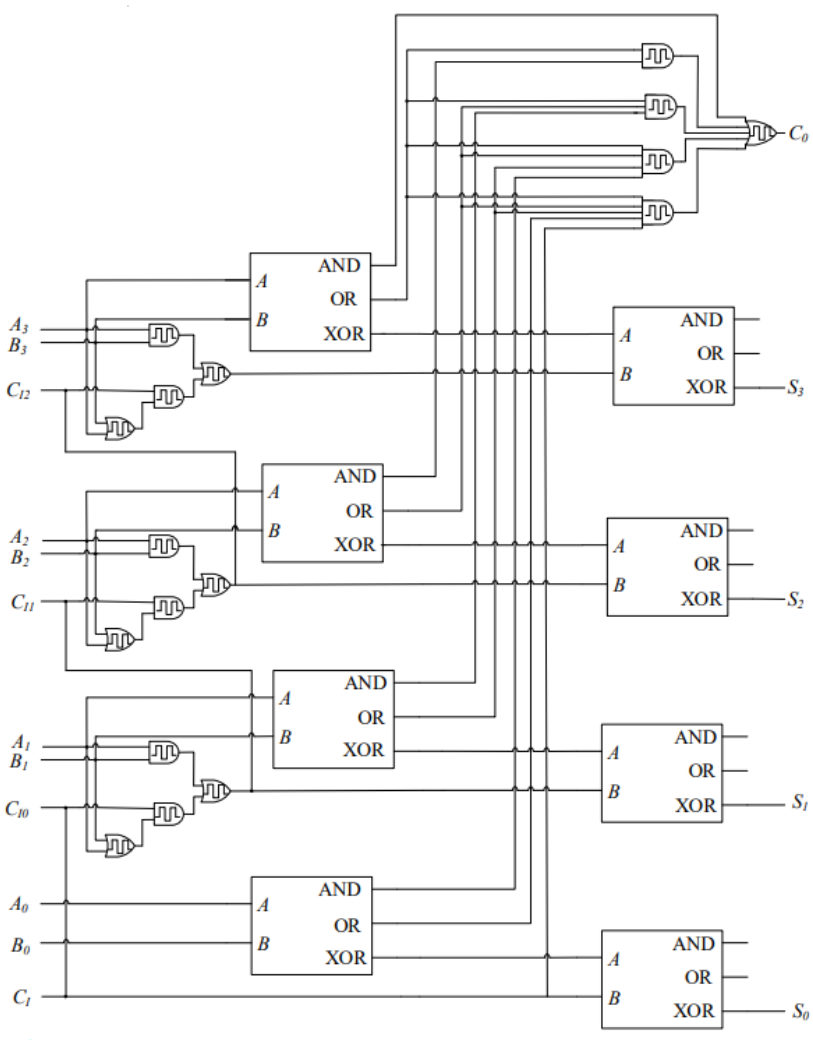

Fig. 11 Enhanced CLA based on MRL

Simulations for improved carry-lookahead adder carried out in LTSPICE. A memristor model that was proposed in [11] is the foundation for the memristor that is used in the circuit. The model has the following parameters: Vp = 0.16V, Vn = 0.15V, Ap = 4000, An = 4000, xp = 0.3, xn = 0.5, p = 1, a1 = 0.17, a2 = 0.17, b = 0.05, and x0 = 0.11. Fig. 12 depicts the simulation results of 4 bit CLA. Redesigning the carry-lookahead adder with the ULG structure can drastically cut down on the number of memristors, simplify the circuit design, and thus lower the power consumption of the circuit.

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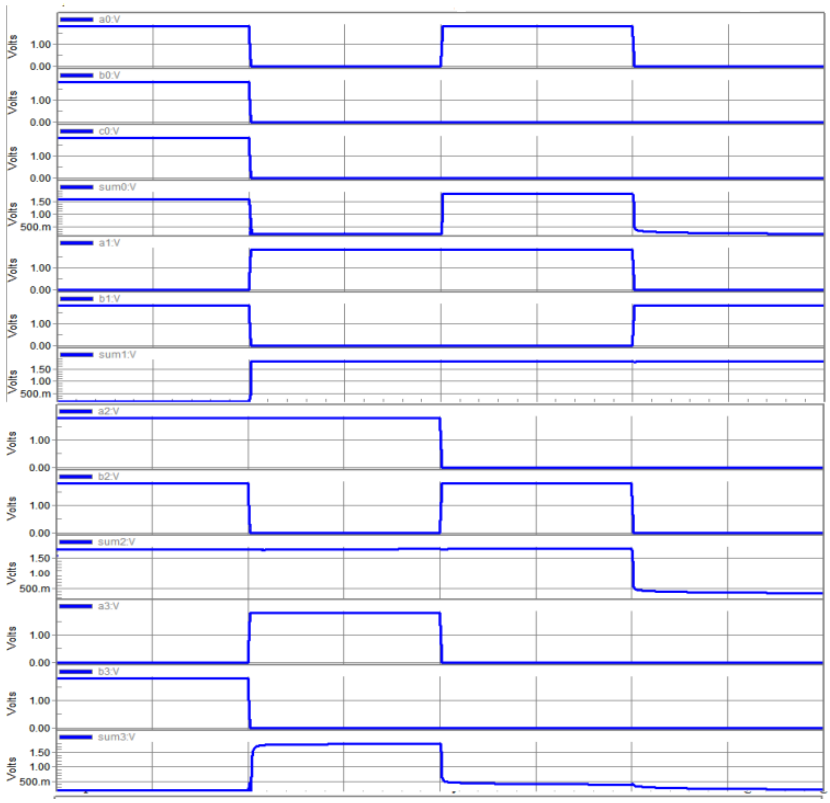

Fig. 12 Simulation results of 4-bit Carry Look–Ahead Adder

Table 1 displays the performance comparisons of the MRL-based, IMP-based, and enhanced CLAs reported.

Table 1 Comparison of Enhanced CLA based on MRL with other technologies

CLA	No. of Memristors	No. of CMOS
Enhanced MRL	76	80
MRL	108	96
IMP	88	-
CMOS	-	248

To be compatible with conventional CMOS circuits, the proposed MRL-based CLAs, however, use the voltage as a logic variable, with high voltage and low voltage denoting logic variables "1" and "0," respectively. The initialization of the memristors and the reading/writing circuit are also not necessary for the MRL-based CLAs.

On the other hand, the suggested CLA uses less memristors than the IMP-based CLA, which is the case. The CMOS is 180 nm in size, compared to the memristor's size of roughly 3 nm. The chip area overhead of the MRL-based circuit is significantly lower than that of the CMOS-based circuit

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because a MOSFET in the logic circuit of the MRL design can fully accept several memristors in terms of technology. The chip area of the enhanced CLA is the smallest when compared to the other two CLAs, as shown in Table 1, because the number of memristors and CMOSs employed is even less than in the MRL-based CLA.

VI. CONCLUSION

This research suggests two conventional CMOS-compatible 4-bit carry look-ahead adders that are based on MRL circuitry. Based on this, a better CLA is created using ULGs, which considerably reduces the number of memristors and CMOS, as well as the chip area and power consumption. The designed circuits are simulated using LTSPICE, and the outcomes match what was anticipated. The design can also be expanded to include a multi-bit carry look-ahead adder.

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